UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/853,005	05/09/2001	Chau-Chad Tsai	JCLA5312	5161

7590 03/13/2003

J C PATENTS INC
4 Venture
Suite 250
Irvine, CA 92618

EXAMINER	
BAKER, PAUL A	
ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 03/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/853,005	TSAI ET AL.	
	Examiner	Art Unit	
	Paul A Baker	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted (Taiwan 89111825) under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Acknowledgment is made of applicant's claim for priority under 35 U.S.C. 119(a)-(d) based upon an application 87119245 filed in Taiwan on 20 November 1998. A claim for priority under 35 U.S.C. 119(a)-(d) cannot be based on said application, since the United States application was filed more than twelve months thereafter.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1, 2, 4 – 6 is rejected under 35 U.S.C. 102(e) as being anticipated by Ziegler et al. US Patent 6,182,176.

In regards to claim 1, Zeigler discloses a cache system inside the peripheral device interface control chip (figure 2 element 116) of a computer system that includes

a memory unit (figure 2 element 115), a central processing unit (CPU) (figure 2 element 120), a CPU bus (figure 2 element 112), a peripheral bus device (figure 2 element 160), comprising:

A data buffer located within the control chip for holding a data stream read from the memory unit so that data required by the peripheral device bus are provided (figure 2 element 166), and when the data stream is synchronous (applicant interprets "synchronous" to mean "coherent with memory" this fits more closely with the applicant's disclosure) with data in a corresponding address within the memory unit (column 4 lines 30 – 42), the data stream is retained, and when any one of the peripheral devices demands data already in the data stream, data within the data stream can be immediately provided by the data buffer so a latency period for retrieving the data stream from memory again is reduced is inherent since a data stream present on the queue (figure 2 element 166) will be ready for transmission when requested by I/O bus (figure 2 element 166); and

a peripheral device interface controller installed within the control chip for determining if the data stream includes data demanded by a particular peripheral device and determining if the data stream is synchronous with data in the corresponding address, then retrieving the data stream from the memory unit and putting the data in a data buffer, and finally switching a state of that portion of the data buffer having data stream therein (figure 2 controller sub-element within element 114).

In regards to claim 2, Zeigler discloses the peripheral device interface controller further includes transmitting a probe-hit-read signal to the central processing unit in column 9 lines 21 – 23.

In regards to claim 4, Zeigler discloses the peripheral device interface controller further includes receiving signals emitted when data are written from the CPU bus to the corresponding address in column 6 line 66 through column 7 line 20.

In regards to claim 5, Zeigler discloses the peripheral device interface controller further includes receiving signals emitted when data are read from the corresponding address to the CPU bus.

In regards to claim 6, Zeigler discloses the data buffer comprises at least one line (figure 2 element 166) caches require the existence of at least one line.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 7 – 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ziegler et al. US Patent 6,182,176.

In regards to claim 3, Zeigler does not disclose the peripheral device interface controller further includes receiving signals emitted when data are written from the peripheral device bus to the corresponding address. However it is well known in the art the necessity indicating the completion of an I/O operation, the two primary means of doing so are the assertion of an signal and the alteration of a special status register, the former is used when the information must be transmitted between modules and the latter is typically used in intra-module communication and also involves a signal asserted but that signal is stored so that a processor may check the status at a latter point in time. Both means of communicating the writing of data from the peripheral device bus to a corresponding address involve the assertion of a signal. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a signal emitted when data is written from the peripheral device bus to the corresponding address for the purpose of notifying the action's completion.

In regards to claim 7, Zeigler does not disclose the data buffer has altogether eight lines. However, the choice of the depth of the data buffer is matter of design, and the exact number is relatively arbitrary (the choice of a larger buffer reduces the likelihood of a cache miss, while the choice of a smaller buffer reduces the physical size and cost of the system). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to set the depth of the data buffer to

eight lines for the purpose of limiting the amount of memory required for the implementation of the data buffer.

In regards to claim 8, Zeigler does not disclose the eight lines are divided into four transmission blocks each having two lines. However it is well known the use of direct mapping caching scheme for placing data objects within a cache. Peripherals on the I/O bus have a unique identifier (address) the use the well known 2-way direct mapped caching scheme (depth of four) would result in four transmission blocks each having two lines. Zeigler does not disclose the exact means of placement of data within a cache block suggesting a plurality of possible schemes. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the eight lines divided into four transmission blocks for the purpose of reducing the complexity of placement logic.

In regards to claim 9, Zeigler does not disclose each line comprises of 32 bytes. However, it is well known in the art that the cache line has a power of two width so that the least significant bits of an address provide an index into the cache line. The currently most popular cache line widths are 32 and 64 bytes. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to comprise each line of 32 bytes.

Claims 10, 12, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ziegler et al. US Patent 6,182,176, in view of Handy "The Cache Memory Book".

In regards to claim 10, Ziegler discloses method of synchronization data transmission between cache memory inside a peripheral device interface control chip (figure 2 element 116) and external device that can be applied to a computer system having a memory unit (figure 2 element 115), at least one central processing unit (figure 120 element 120), a control chip (figure 2 element 114), a peripheral device bus (figure 2 element 160), a CPU bus and at least one peripheral device (figure 2 element 112), a memory data stream becomes a cache data stream when the memory data stream within the memory is read into the central processing unit, and the memory data stream becomes a buffer data stream when the memory data stream is read into the data buffer (figure 2 element 166).

Zeigler does not disclose the control chip includes a peripheral device interface controller and a data buffer and the central processing unit uses a MOESI protocol, and

when the cache data stream is in a modified state and if the data buffer executes a read operation from an address in memory that corresponds to the cache data stream, the peripheral device interface controller inform the central processing unit to set the cache data stream into an owner state; and

when the cache data stream is in an exclusive state and if the data buffer executes a read operation from the corresponding address, the peripheral device interface controller will inform the central processing unit to set the cache data stream into a shared state.

Handy discloses the MOESI protocol on page 165 – 169, while Zeigler does not directly disclose the exact protocol for maintaining coherency in the cache, MOESI is one of the two most popular protocols implemented in the current state of the art. The disclosure of snooping (column 4 lines 33 – 38) which is necessary for the implementation of the MOESI protocol suggests Zeigler's disclosure is sufficiently enabled to implement the MOESI protocol. Handy also discloses in table 4.3 on page 167 under the **From System Bus** heading "Read Hit" row "Modified" column shows that a read hit on a Modified cache line will update the status to Owned, and "Exclusive" column shows that a read hit on an Exclusive cache line will update the status to Shared. With the MOESI protocol implemented within Zeigler this would lead to informing the central processing unit to set the cache data stream to an owner state when the cache data stream is in a modified state and the data buffer executes a read operation from an address in memory that corresponds to the cache data stream, and informing the central processing unit to set the cache data stream into a shared state when the cache data stream is in an exclusive state and if the data buffer executes a read operation from the corresponding address. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the MOESI protocol for the purpose of maintaining cache coherency.

In regards to claim 12, Zeigler discloses a probe-hit-read signal is transmitted from the peripheral device interface controller to the central processing unit when a

buffer data stream is read from the peripheral device interface controller to the data buffer in column 9 lines 21 – 23.

In regards to claim 13, Zeigler does not explicitly disclose the probe-hit-read signal further includes the corresponding addresses however the CPU needs to know where the data stream is located within the data buffer. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the corresponding address for the purpose of notifying the CPU the location on the data stream.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ziegler et al. US Patent 6,182,176, in view of Handy "The Cache Memory Book", in further view of Islam et al. US Patent 6,032,228.

Zeigler discloses a cache coherency and replacement strategy without specifying which protocol and Handy discloses a particular cache coherency scheme.

Handy further discloses the data buffer is set to an empty state on initialization on page 48 2nd paragraph;

Neither Zeigler nor Handy disclose:

when the peripheral device interface controller reads the buffer data stream into the data buffer according to the requirement of the particular peripheral device, a buffered data portion of the data buffer that includes the buffer data stream is set to a clean-unaccessed state;

when the buffered data portion is in a clean-unaccessed state and if the peripheral device interface controller detects from the CPU bus a write or a read operation using the corresponding address, the buffered data portion is set to a dirty unaccessed state;

when the buffered data portion is in the clean-unaccessed state, if the peripheral device interface controller detects from the peripheral device bus a write operation using the corresponding address, the buffered data portion is set to a dirty-unaccessed state;

when the buffered data portion is in the clean-unaccessed state and if the particular peripheral device that demands the buffer data stream reads the buffer data stream from the buffered data portion, the buffered data portion is set to a clean-accessed state;

when the buffered data portion is in a dirty-unaccessed state and if the particular peripheral device that demands the buffer data stream reads the buffer data stream from the buffered data portion, the buffered data portion is set to an empty state;

when the buffered data portion is in a clean-accessed state and if the peripheral device interface controller detects from the CPU bus a read or a write operation using the corresponding address, the buffered data portion is set to an empty state; and

when the buffered data portion is in the clean-accessed state and if the peripheral device interface controller detects from the peripheral device bus a write operation using the corresponding address, the buffered data portion is set to an empty state.

Islam discloses a cache coherency scheme capable of implementing virtually any cache coherency and cache replacement strategy (column 1 lines 41 –45). Islam discloses the use of two status bits accessed and dirty in column 4 lines 52 – 64. The dirty bit is associated with non-owners accessing the data buffer. The accessed bit is associated with the owner accessing the data buffer. When an owner (peripheral device) reads a buffered data stream into the data buffer, the data has neither been accessed nor modified so its status would be clean-unaccessed (figure 1c 1st column). When a clean-unaccessed data buffer is read or written to by the non-owner (CPU) the data has been modified and the state of the buffer is changed to dirty-unaccessed (figure 1c 2nd column). When a clean-unaccessed data buffer is read from the owner (peripheral device) the buffer has been accessed and the status of the buffer is transferred to the clean-accessed (figure 1c 3rd column) state. When a dirty-unaccessed data buffer is read from the owner (peripheral device) the data has been accessed, since the peripheral device has no further use of the buffer the state is changed to invalid (empty). When the clean-accessed data buffer is accessed either by the CPU or peripheral device, the contents of the data buffer are stale (the data has already been transferred by the peripheral device) and therefore are invalidated (set to empty). While Islam does not fully restrict the state changes as stated above (for instance Islam also discloses a dirty-accessed state available if the protocol requires use of it) the state transitions described above are generally accepted when access and dirty bits are used in cache coherency.

Inclusion of Islam's general cache coherency scheme (a superset of Handy's MOESI protocol) would provide support for Handy's protocol and would satisfy Zeigler's stated use of a cache coherency mechanism. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Islam's cache coherency and cache replacement strategy into Zeigler and Handy for the purpose of maintaining cache coherency.

Claims 14 - 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ziegler et al. US Patent 6,182,176, in view of Islam et al. US Patent 6,032,228

In regards to claim 14, Zeigler discloses a method of synchronization data transmission between cache memory inside a peripheral device interface chip (figure 2 element 166) and external device that can be applied to a computer system having a memory unit (figure 2 element 115), at least one central processing unit (figure 2 element 120), a control chip (figure 2 element 114), a peripheral device bus (figure 2 element 160), a CPU bus (figure 2 element 112) and at least one peripheral device (inherent), wherein the control chip includes a peripheral device interface controller (figure 2 element 114 sub-element controller) and a data buffer (figure 2 element 166), and a data stream becomes a buffer data stream when the memory data stream inside the memory is read into the buffer data. Zeigler discloses a cache coherency and replacement strategy without specifying which protocol.

Zeigler does not disclose:

setting the data buffer to an empty state on initialization;

setting the buffered data portion of the data buffer that includes the buffer data stream to a clean-unaccessed (figure 1c 1st column) state when the peripheral device interface controller reads the buffer data stream into the data buffer according to the requirement of the particular peripheral device;

setting the buffered data portion to a dirty-unaccessed (figure 1c 2nd column) state if the peripheral device interface controller detects from the CPU bus a write or a read operation using the corresponding address when the buffered data portion is in a clean-unaccessed state;

setting the buffered data portion to a dirty-unaccessed state if the peripheral device interface controller detects from the peripheral device bus a write operation using the corresponding address when the buffered data portion is in the clean-unaccessed state;

setting the buffered data portion to a clean-accessed (figure 1c 3rd column) state if the particular peripheral device that demands the buffer data stream, reads the buffer data stream from the buffered data portion when the buffered data portion is in the clean-unaccessed state;

setting the buffered data portion to an empty state if the particular peripheral device that demands the buffer data stream, reads the buffer data stream from the buffered data portion when the buffered data portion is in a dirty-unaccessed state;

setting the buffered data portion to an empty state if the peripheral device interface controller detects from the CPU bus a read or a write operation using the corresponding address when the buffered data portion is in a clean-accessed state;

and setting the buffered data portion to an empty state if the peripheral device interface controller detects from the peripheral device bus a write operation using the corresponding address when the buffered data portion is in the clean-accessed state.

A cache line is always set to invalid (empty) upon initialization.

Islam discloses a cache coherency scheme capable of implementing virtually any cache coherency and cache replacement strategy (column 1 lines 41 –45). Islam discloses the use of two status bits accessed and dirty in column 4 lines 52 – 64. The dirty bit is associated with non-owners accessing the data buffer. The accessed bit is associated with the owner accessing the data buffer. When an owner (peripheral device) reads a buffered data stream into the data buffer, the data has neither been accessed nor modified so its status would be clean-unaccessed. When a clean-unaccessed data buffer is read or written to by the non-owner (CPU) the data has been modified and the state of the buffer is changed to dirty-unaccessed. When a clean-unaccessed data buffer is read from the owner (peripheral device) the buffer has been accessed and the status of the buffer is transferred to the clean-accessed state. When a dirty-unaccessed data buffer is read from the owner (peripheral device) the data has been accessed, since the peripheral device has no further use of the buffer the state is changed to invalid (empty). When the clean-accessed data buffer is accessed either by the CPU or peripheral device, the contents of the data buffer are stale (the data has

already been transferred by the peripheral device) and therefore are invalidated (set to empty). While Islam does not fully restrict the state changes as stated above (for instance Islam also discloses a dirty-accessed state available if the protocol requires use of it) the state transitions described above are generally accepted when access and dirty bits are used in cache coherency.

Inclusion of Islam's general cache coherency scheme would satisfy Zeigler's stated use of a cache coherency mechanism. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Islam's cache coherency and cache replacement strategy into Zeigler for the purpose of maintaining cache coherency.

In regards to claim 15, Zeigler discloses a probe-hit-read signal is transmitted from the peripheral device interface controller to the central processing unit when a buffer data stream is read from the peripheral device interface controller to the data buffer in column 9 lines 21 – 23.

In regards to claim 16, Zeigler does not explicitly disclose the probe-hit-read signal further includes the corresponding addresses however the CPU needs to know where the data stream is located within the data buffer. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the corresponding address for the purpose of notifying the CPU the location on the data stream.

Response to Amendment

The examiner mistakenly referred to the buffer element 162 of Figure 2 in claim 1 when the intent was to refer to cache element 166, the cache element permits immediately access to data already in the data stream.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A Baker whose telephone number is (703)305-3304. The examiner can normally be reached on M-F 10am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do Yoo can be reached on (703)308-4908. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7238 for regular communications and (703)746-7240 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Reginald G. Bragdon

REGINALD G. BRAGDON
PRIMARY EXAMINER

PB
March 10, 2003